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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MCDONALD, SHANTESE L

ART UNIT

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GROUP 3700

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/074,345
Filing Date: February 12, 2002
Appellant(s): TAM ET AL.

Keith M. Tackett
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/28/06 appealing from the Office action
mailed 5/24/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,544,892	Srinivasan et al.	4-2003
6,599,174	Spikes, Jr.	7-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-25 and 30-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan et al. in view of Spikes, Jr.

Srinivasan et al. teaches a method of removing a dielectric disposed on a substrate, having a first dielectric, which is silicon oxide, and a second dielectric material, which is silicon nitride, disposed thereon, (col. 8, lines 46-49), comprising positioning the substrate in proximity with a fixed abrasive polishing pad, (col. 8, lines 21-25), dispensing a polishing composition having at least one organic compound, which comprises an amino acid which comprises glycine in about 0.01 to about 20 wt. % of the polishing composition, (col. 6, lines 27-30), an also praline, (col. 10, line 10), at least one pH adjusting agent, which is potassium hydroxide, deionized water, and combinations thereof, (col. 6, lines 31-45), and the pH of the composition is between 9 and 12, (col. 7, lines 20-34), Srinivasan et al. also teaches that the substrate includes a

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shallow trench isolation structure, (col. 6, lines 50-53), and chemical mechanical polishing the substrate wherein the at least one organic compound enhances the removal rate of the first dielectric material using the fixed abrasive polishing pad without affecting the removal rate of the second dielectric material, (col. 6, line 60 – col. 7, line 7), and the second removal rate being less than the first removal rate. Srinivasan et al. teaches all the limitations of the claims except for pre-polishing the substrate to planarize the substrate by removing a bulk overfill of the first dielectric material, the polishing system comprising a carousel with at least one substrate head assembly, a controller, a first and second platen and removing the silicon nitride at a rate of between about 0.01 to about 300 Å/min, removing the silicon oxide at a rate of between about 50 and 5000 Å/min, and the silicon oxide and the silicon nitride being removed at a removal rate ratio of greater than 10:1 and from about 100:1 to about 2000:1 Spikes Jr. et al. teaches a carousel, 40, a controller, 28, first and second platens, (col. 8, lines 58-61), pre-polishing the substrate, (col. 8, lines 36-37). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the polishing method of Srinivasan et al. with a pre-polish step, a carousel, first and second platens and a controller, in order to remove the bulk overfill of dielectric material and more efficiently polish the substrates.

It would have been further obvious to one having ordinary skill in the art at the time the invention was made, to provide the polishing system with a the capability to remove the silicon nitride at a rate of between about 0.01 to about 300 Å/min, removing the silicon oxide at a rate of between about 50 and 5000 Å/min, and the silicon oxide

and the silicon nitride being removed at a removal rate ratio of greater than 10:1 and from about 100:1 to about 2000:1, in order to vary outcome of the polishing dependant on the desired end product.

(10) Response to Argument

The Applicant argues that there is no motivation or teaching to combine the Srinivasan et al. and the Spikes, Jr. reference. The Examiner disagrees. Both references teach a multiple polishing procedure for removing dielectric material disposed on a substrate, using a fixed abrasive and a polishing solution. The Spikes, Jr. reference teaches that typically CMP is used to planarize a non-uniform polishing surface of a process layer and CMP may be used to reduce surface variations in a pre-polish step, (col. 1, lines 56-67). Therefore the Spikes, Jr. reference was cited and teaches that a pre-polish step during the planarization of a substrate with dielectric polishing layers, and during a polishing procedure with multiple polishing steps, is a known procedure in the art.

The Applicant is further arguing that Srinivasan et al. teaches a one step polishing method and does not disclose a pre-polishing step and that the Spikes, Jr. discloses a two step polishing process wherein the first polishing step a slurry is provided to the polishing pad to remove material from the layer, and a second polishing process which is substantially slurryless. The Applicant also argues that there is not teaching to have slurry present for the second polishing step of Spikes, Jr. and that Spikes, Jr. does not teach a pre-polish step. The Applicant states that the Examiner has stated that rather than using the one step polishing process taught by Srinivasan et al.

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al., one of ordinary skill in the art, when confronted with Spikes, Jr., would perform multiple step process taught by Spikes, Jr., while using the amino acid in the polish slurry taught by Srinivasan et al.

The Examiner disagrees with the above listed arguments. The Examiner notes that Spikes, Jr. does teach a pre-polish step, (col. 8, lines 36-37). The Examiner further disputes the Applicant's arguments, and notes that the Spikes, Jr. reference was not cited as a teaching for replacing the polishing method step in which no slurry was utilized with the polishing step of Srinivasan et al. The Spikes, Jr. reference was cited to teach a pre-polish step, for removing a bulk overfill of dielectric material is a known practice in the art, and one of ordinary skill in the art would/could perform a pre-polish step before the polishing method as taught by Srinivasan et al.


(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

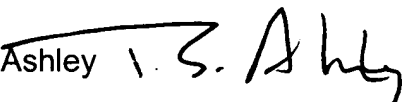
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